ABSTRACT

A process and a device are proposed for testing a serializer and deserializer circuit arrangement (2, 3), where to control the test sequence a simple digital interface (12) is used. To test the serializer circuit arrangement (2) firstly the quality of a multiphase clock signal (CLK) of the serializer circuit arrangement (2) and secondly the ability to transmit a preset bit pattern are tested. To test the deserializer circuit arrangement (3) the quality of the multiphase clock signal (CLK) and the quality of a data eye obtained during clock and data recovery are tested together with the quality of the clock recovery.